REMARKS

This responds to the Office Action mailed on February 28, 2006. Claims 1, 8, 15 and 21 are amended. Claims 1-23 are pending in this application.

§112 Rejection of the Claims

Claims 1-23 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1-23 were also rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Both rejections were based on the claim limitation "creating bypass logic in a digital circuit design that is without bypass logic."

Applicant has amended claims 1, 8, 15 and 21 to overcome both rejections under 35 USC § 112. In particular, Applicant has replaced the phrase "creating a bypass logic" with the phrase "adding a bypass logic." Further, Applicant has removed the limitation of "without bypass logic." Claims 8, 15 and 21 include similar amendments. Such amendments are at least supported by Figures 1-2 and the detailed description at ¶16. Therefore, Applicant respectfully requests that both rejections of claims 1-23 under 35 USC § 112 be withdrawn.

§102 Rejection of the Claims

Claims 1-3, 5, 8-11, 15-17, and 21 were rejected under 35 USC § 102(b) as being anticipated by Vashi (U.S. 6,219,819). Applicant respectfully traverses the rejection. Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration.[1]

The Office indicated that

> the limitation "creating bypass logic in a digital circuit design that is without bypass logic" in the preamble of the claim is not given patentable weight . . .[2]

Applicant respectfully traverses this assertion. This limitation is in the body of the claim. Specifically, the limitation is after the transitional phrase "comprising" and the colon. Accordingly, this limitation is given patentable weight.

The Office also indicated that

> Vashi does disclose creating bypass logic in a digital circuit design that is without bypass logic, wherein creating comprising transforming a conditional state element into a logically redundant element in the digital circuit design. (emphasis added) [3]

Applicant respectfully traverses this assertion. The Office does not indicate where the limitation of "transforming of a conditional state element into a logically redundant element" is disclosed in Vashi. Applicant respectfully submits that Vashi does not disclose the transforming of a conditional state element into a logically redundant element. Accordingly, because the cited reference does not disclose all of the claim limitations, Applicants respectfully submit that the rejection of claims 1, 8, 15 and 21 under 35 U.S.C. §102 has been overcome. Claims 2-3, 5; claims 9-11 and claims 16-17 depend from, respectively, claims 1, 8 and 15 and distinguish the reference for at least the same reason.

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[1] *In re Dillon* 919 F.2d 688, 16 USPQ2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991).
[2] Office Action at ¶8.
[3] Office Action at ¶8.

§103 Rejection of the Claims

Claims 22-23 were rejected under 35 USC § 103(a) as being unpatentable over Vashi (U.S. 6,219,819) in view of McFarland (U.S. 6,212,629). Because claims 22-23 depend from and further define claim 21, Applicant respectfully submits that the rejection of claims 22-23 under 35 U.S.C. §103 has been overcome.

Allowable Subject Matter

Claims 4, 6-7, 12-14, and 18-20 were indicated to be allowable if rewritten to overcome the rejection(s) under 35 USC § 112, second paragraph, set forth in the Office Action. Applicant acknowledges the allowable subject matter.

The Office Action indicated reasons for allowable subject matter. The Office Action uses the term "prior art." However, Applicant does not make any admissions regarding the prior-art status of any references in the record of the application. Instead, Applicant regards these references as only being "of record." Additionally, Applicant submits that the Office Action makes numerous assertions regarding the interpretations of limitations of the claims, the contents of the art and distinguishing features of the claims. Applicant has neither verified nor accepted the accuracy of these assertions, and respectfully submits that there may be different interpretations that those identified in the Office Action. Additionally, Applicant respectfully submits that the relevant claims may be allowable for one or more reasons in addition to and/or in alternative to those reasons identified in the Office Action. Applicant reserves the right to further address one or more aspects of the reasons for allowance as may later be necessary or desirable.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 371-2103 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 24th day of April, 2006.

Amy Moriarty
Name

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Signature